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METHOD FOR FORMING A POSITION ALIGNMENT MARK USED FOR ELECTRON BEAM EXPOSURE

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A METHOD FOR FORMING POSITION ALIGNMENT MARK USED FOR ELECTRON BEAM EXPOSURE

[Denshi biimu roko yo ichi awase maaku no keisei hoho]

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[There are no amendments to this patent.]

Claims

1. A method for forming a position alignment mark used for electron beam exposure, characterized in that it contains a process that successively layers a thin film and a first resist film on top of a semiconductor substrate on which an activation layer has been formed on one of the faces, a process that forms a first aperture at a position corresponding to a section in which the above-mentioned activation layer for this first resist film has been formed and a second aperture

an ohmic electrode and a metallic film used for a position alignment mark on top of the

above-mentioned active layer and the above-mentioned semiconductor substrate by passing through the above-mentioned thin film that was removed by etching, a process that forms, on top of the above-mentioned thin film, a second resist film having a third aperture containing a metallic film used for the above-mentioned position alignment mark after the above-mentioned first resist film is removed, and a process that, after removing the above-mentioned metallic film used for the above-mentioned position alignment mark by using the above-mentioned thin film as a mask, removes the above-mentioned semiconductor substrate by etching.

2. A method for forming a position alignment mark used for electron beam exposure as recorded in Claim 1, characterized in that a position alignment mark of a concave shape is formed on the above-mentioned semiconductor substrate by means of forming in one place a second aperture that is formed on the above-mentioned first resist film

3. A method for forming a position alignment mark used for electron beam exposure as recorded in Claim 1, characterized in that, by means of creating, in two locations, second apertures on the above-mentioned first resist film concave sections that is formed on the above-mentioned semiconductor substrate, a convex position alignment mark is formed by means of the above-mentioned semiconductor substrate which is not removed that is sandwiched between this concave section and these concave sections at two locations.

Detailed explanation of the invention

Objective of the invention

Industrial application field

This invention relates to a method for forming a position alignment mark used for electron beam exposure in the manufacture of semiconductor devices.

Prior art

The minimum processing dimensions that are required in the manufacturing processes for a semiconductor device are extremely minute, and the minimum gate electrode dimensions for a microwave semiconductor device using chemical semiconductors such as gallium arsenic (GaAs) have already passed 0.25 μm. Electron beam exposure technology using an electron beam is being widely used as a processing method for this type of microscopic pattern.

For the position alignment mark that is necessary for the purpose of forming a pattern on

[illegible]

of the detection signal are greatly affected by the forming conditions for this position alignment mark. As for the conditions required for the position alignment mark used for electron beam

exposure, it is most important that the edge sections of the mark be cut sharply and that the surface of the concave mark or the convex mark be smooth.

However, in electron beam exposure, because a long time is required in exposure, the throughput is poor compared to ordinary optical exposure at the time of manufacturing a semiconductor device, and there are frequently cases in which it is only used in processes in which the most precise processing is required. For example, in a Schottky barrier type field effect transistor using a GaAsFET (MESFET), generally, electron beam exposure is used in the pattern forming for the gate electrode, and for the other processes, pattern forming is conducted by light exposure.

The characteristics of MESFET are significantly influenced by the dimensions of the gate electrode and the separation of the source electrode and drain electrode, which are ohmic electrodes. Therefore, the position alignment of the gate electrode of the MESFET must be conducted with good precision in contrast to the ohmic electrode. Because of this, it is desired that the posistion alignment mark used for the electron beam exposure that is used in a MESFET be formed at the same time as the forming of the ohmic electrodes.

However, with the ohmic electrode of the MESFET, generally, an alloy comprising Ni and AuGe is used, and in order to obtain an ohmic connection with the semiconductor substrate, the alloying process is conducted at a high temperature of 450°C or more. Because of this, in the event the position alignment mark used for the electron beam exposure is formed from Ni and AuGe, there is a deterioration of the edge section of the position alignment mark and a severe loss of the smoothness of the surface because of the alloying process for the ohmic electrode.

Therefore, even if the position alignment mark used for the electron beam exposure is formed at the same time as the ohmic electrode, the position detection precision and the S/N ratio of the detection signal that can be obtained by means of the electron beam radiation is insufficient for the required value. In addition, the surface condition of the position alignment becomes completely changed just by the slight differences in the composition of the Ni and the AuGe, and by conditions such as temperature and time at the time of alloying changing slightly, and in severe cases, the noise component of the detection signal becomes too large, and there are cases in which mark detection becomes impossible.

Also, when the ohmic electrode and the position alignment mark used for the electron beam are patterned separately, and the position alignment mark used for the electron beam does

brought about.

Problems to be solved by the invention

As was explained above, in the method for forming a position alignment mark used for electron beam exposure that was used in the past, the position alignment mark was deformed due to the thermal heat treating process at the time of the formation of the ohmic electrode, and the position alignment of the gate electrodes could not be accurately done. Thus, with this invention, this type of defect is eliminated, and the objective is to form a position alignment mark in which accurate position alignment of the gate electrodes can be conducted.

Constitution of the invention

Means to solve the problems

In order to achieve the above-mentioned objective, with the method for forming a position alignment mark used for electron beam exposure of this invention, a thin film is formed having a first aperture used for the ohmic electrodes and a second aperture used for the position alignment mark formation on top of a semiconductor substrate, the metallic film used for the ohmic connection passes through the first aperture and is coated on the semiconductor substrate, and the position alignment mark is formed by means of etching away a section of the semiconductor substrate through the second aperture.

Operation

In the method for forming a position alignment mark used for electron beam exposure of this invention, a step is formed in the semiconductor substrate by means of etching away a section of the semiconductor substrate; this step is made a position alignment mark, and since thermal deformation of the semiconductor substrate is difficult to bring about with the thermal processing that accompanies the alloying process during the ohmic electrode formation, the position alignment mark is not deformed. Also, since the forming position for the position alignment mark is conducted at the same time as setting the forming position for the ohmic electrodes, in the event the gate electrodes are formed by using the position alignment mark as a target, positional mismatch of the ohmic electrode and the gate electrode is eliminated.

Application examples

Below, an explanation is given for one application example of this invention with [illegible] manufacturing method for [illegible] exposure of this invention [illegible] layer (2) is formed on top of the semiconductor substrate (1), for example, a semi-insulating

GaAs substrate, on top of this semiconductor substrate (1), a thin film, for example, a 3000 Å SiO_2 film (3), and a resist film (4), are successively accumulated.

Next, as is shown in Figure 1(b), in order to remove the SiO_2 film (3) by etching, a first aperture (5) and a second aperture (6) are formed in the resist film (4). Here, the first aperture (5), in order to form the source electrode and the drain electrode, which are ohmic electrodes, is formed in two places at positions corresponding to the section at which the activation layer (2) of the resist film (4) is formed. The second aperture (6) is formed in one location at a position corresponding to the section at which the activation layer of the resist film (4) is not formed in order to form the position alignment mark. After that, using the resist film (4) as a mask, the exposed SiO_2 film (3) is removed by etching at the same time.

Next, as is shown in Figure 1(c), the metallic film that is formed by Ni-AuGe is deposited to 2000 Å on top of the activation layer (2) and the semiconductor substrate (1) through the first aperture (5) and the second aperture (6). Here, the metallic film that is deposited through the first aperture becomes the metallic film (7-1) used for the ohmic electrodes, and the metallic film that is deposited through the second aperture becomes the metallic film (7-2) used for the position alignment mark. Then, the unwanted sections of the metallic film are removed along with the resist film by using a lift-off method.

Next, as is shown in Figure 1(d), a resist film (8) is newly painted on the semiconductor substrate (1), and the third aperture is formed including the metallic film (7-2) used for the position alignment mark. Then, after the metallic film (7-2) used for the position alignment mark within the third aperture (9) is removed and the semiconductor substrate (1) face is exposed, the exposed face of the semiconductor substrate (1) is etched by using the SiO_2 film (3) as a mask, and the concave position alignment mark (10) is formed.

Next, as is shown in Figure 1(e), the SiO_2 film (3) is peeled off and the ohmic electrode (11) is formed by means of an alloying process, and finally, position alignment of the gate electrodes is conducted using the position alignment mark (10) as a target by means of electron beam exposure, and by means of forming the gate electrode (12), the MESFET is completed.

As for the position alignment mark (10) used for electron beam exposure that was obtained in this manner, since it is not influenced in any way by the thermal process that accompanies the alloying process during the ohmic electrode formation because it is directly formed on the semiconductor substrate (1), excellent signal detection for the gate electrode can

[illegible] almost the same as the design value.

In the explanation of Figure 1, an example of a convex shape was explained as the cross-sectional shape of the position alignment mark used for electron beam exposure, but the formation of a concave position alignment mark is also possible. In other words, in the process of Figure 1(b) of Application Example 1, a second aperture (6') is provided in two locations in the section in which the activation layer (2) is not formed on top of the semiconductor substrate (1) for the resist film (4) at the same time as providing the first aperture (5). Next, the SiO_2 film (3) is removed by etching by using this resist film (4) as a mask. Then, after a metallic film is covered on the entire face of the semiconductor substrate (1), if the resist film (4) and the unwanted metallic film are removed by using a lift-off method, as is shown in Figure 2(a), the metallic film (7-1) used for the ohmic electrode and the metallic film (7-2') used for the position alignment mark are respectively formed in two locations on top of the activation layer (2) and the semiconductor substrate (1) through the SiO_2 film (3) that was removed by etching.

Next, as is shown in Figure 2(b), a resist film (8) is newly painted on the semiconductor substrate (1), and the third aperture (9') is formed including the metallic film (7-2') used for position alignment for two locations. Then, after exposing the semiconductor substrate (1) by etching away the metallic film (7-2') used for position alignment within the third aperture (9'), the concave sections are formed at two locations by means of etching the exposed face of the semiconductor substrate (1) by using the SiO_2 film (3) as a mask. Here, the concave sections for two locations [illegible: probably an adverb] form the convex position alignment mark (10') by means of the non-etched semiconductor substrate (1) sandwiched by the concave sections. Finally, as is shown in Figure 2(c), using the convex position alignment marks (10') as a target, position alignment of the gate electrode is conducted, and the gate electrode (12) is formed.

As for the convex position alignment marks (10') that are formed in this manner, along with their not being influenced by the alloying process at the time of forming the ohmic electrodes in the same manner as the above-mentioned Application Example 1, the position alignment precision becomes high.

In the above-mentioned Application Examples 1 and 2, in regard to the depth of the etching of the semiconductor substrate (1), it is necessary to determine this according to the conditions for the electron beam radiation for the of alignment mark position detection, but even in the case of a comparatively shallow [depth] of about 0.3 mm, a sufficient signal strength can be obtained. Also, for the film thickness of the SiO_2 film (3), it is desirable that it be made the

Also, as for the SiO_2 film, it can be other insulating films, for example, SiO and Si_3N_4, metallic films of Al, Au, or the like, and combinations of these, and the semiconductor substrate

is also not limited to a semi-insulating GaAs substrate. Also, Ni-AuGe was used as an example as the metallic film used for the ohmic electrodes, but it can also be Au-AuGe, or Pt-AuGe, and it does not matter even if it is covered by a metal layer used for a bonding pad made of Au-Pt-Ti on the upper section of the metal layer used for the ohmic electrodes. Also, [this invention] is not limited to electron beam exposure, and of course, can also be used with other electrically charged beam exposure [methods], for example, ion beam exposure.

Effect of the invention

As was explained above, according to this invention, since the position alignment mark is formed directly on the semiconductor substrate, deformation of the position alignment mark does not occur due to the heat treating process that accompanies the alloying process during the ohmic electrode formation. Therefore, an excellent position alignment mark used for electron beam exposure can be formed in which the position detection precision is high, and a detection signal can be obtained in which the noise component is slight.

Brief description of the figures

Figures 1(a) to 1(e) are process cross-sectional views showing one application example of this invention, and Figures 2(a) to 2(c) are process cross-sectional views showing another application example of this invention.

1 Semiconductor substrate
2 Activation layer
3 SiO_2 film
4 First resist film
5 First aperture
6 Second aperture
7-1 Metallic film used for ohmic electrodes
7-2, 7-2' Metallic film used for position alignment mark
8 Second resist film
9, 9' Third aperture
10, 10' Position alignment mark

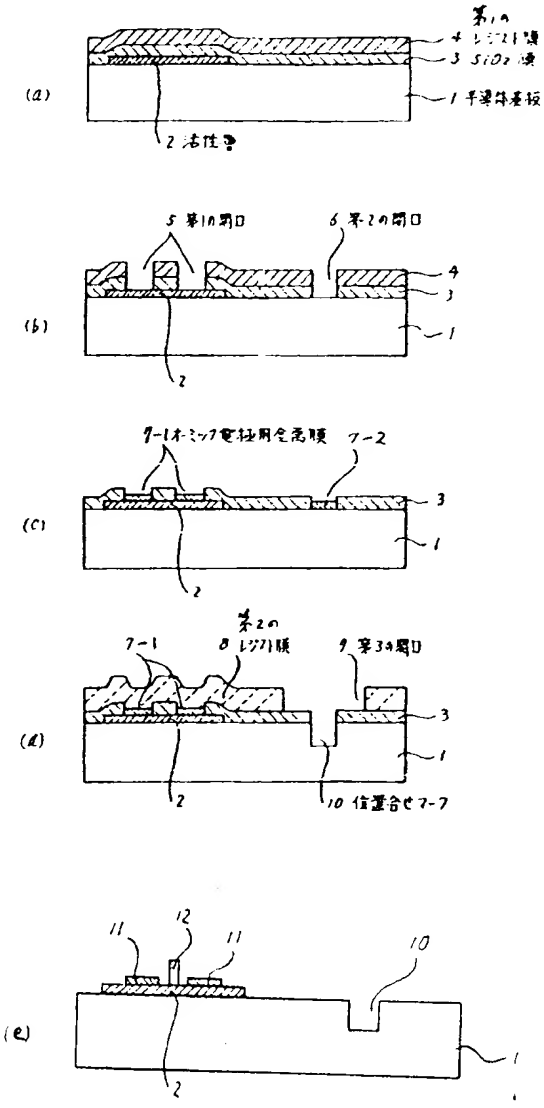

Figure 1

Keys:
1 Semiconductor substrate
2 Activation layer
3 SiO2 film
4 First resist film
5 First aperture
6 Second aperture

10 Position alignment mark

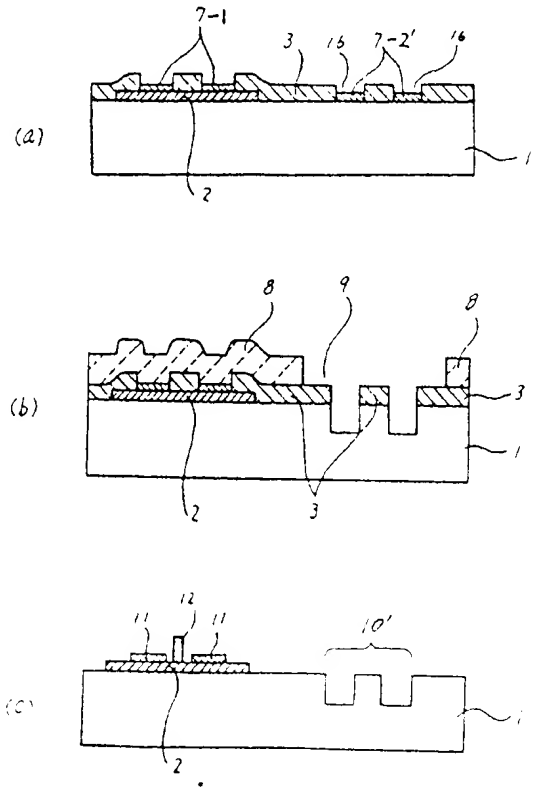

Figure 2

DERWENT-ACC-NO: 1988-259909
DERWENT-WEEK: 198837

TITLE: Mfg. alignment mark for electron beam exposure on substrate - by forming film, having 1st aperture for ohmic contact and 2nd aperture for alignment mark, etc. NoAbstract Dwg 2/2

PATENT-ASSIGNEE: TOSHIBA KK[TOKE]

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ABSTRACTED-PUB-NO:
EQUIVALENT-ABSTRACTS:

TITLE-TERMS:
MANUFACTURE ALIGN MARK ELECTRON BEAM EXPOSE SUBSTRATE FORMING FILM APERTURE OHM CONTACT APERTURE ALIGN MARK NOABSTRACT

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C06B;

EPI-CODES: U11-C04B1; U11-C04B3;

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TITLE: FORMING METHOD FOR ALIGNMENT MARK FOR ELECTRON BEAM EXPOSURE

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US-CL-CURRENT: 438/FOR.435,438/975

ABSTRACT:
PURPOSE: To form a preferable alignment mark for electron beam exposure by removing by etching part of a semiconductor substrate through a second opening on the substrate.

CONSTITUTION: An active layer 2, a thin film 3 and a resist film 4 are sequentially laminated on a semiconductor substrate 1. A first opening 5 and a second opening 6 are formed in the film 4. The opening 5 is formed at the position corresponding to the part not provided with the active layer 2 of the film 4. An ohmic electrode metal film 7-1 and an alignment mark metal film 7-2 are formed through the openings 5, 6. The substrate 1 is covered with a resist

substrate 1 is etched to form a recess alignment mark 10. The film 3 is
separated to form an ohmic electrode 11. With the mark 10 as a target a gate
electrode 12 is formed by positioning it.

⑲日本国特許庁（JP）　　⑪特許出願公開

⑫公開特許公報（A）　　昭63-187628

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H 01 L 21/30	341	K-7525-5F	

審査請求　未請求　発明の数　1　（全5頁）

⑤発明の名称　電子ビーム露光用位置合せマークの形成方法

㉑特　願　昭62-18260

㉒出　願　昭62（1987）1月30日

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明　細　書

1.　発明の名称

電子ビーム露光用位置合せマークの形成方法

2.　特許請求の範囲

(1) 一方の面に活性層が形成された半導体基板上に薄膜及び第1のレジスト膜を順次堆積する工程と、この第1のレジスト膜の前記活性層が形成された部分に対応する位置に第1の開口及び前記活性層が形成されない部分に対応する位置に第2の開口を形成する工程と、前記第1のレジスト膜をマスクにして前記薄膜を除去する工程と、前記エッチング除去された薄膜を通して前記活性層及び前記半導体基板上にオーミック電極用金属膜及び [illegible]

[illegible]

[illegible]スト膜を前記薄膜上に形成する工程と、前記薄膜をマスクにして前記位置合せマーク用金属膜を除[illegible]

[illegible]

位置合せマークの形成方法。

(2) 前記第1のレジスト膜へ形成する第2の開口を1ケ所形成することにより前記半導体基板に凹状の位置合せマークを形成することを特徴とする特許請求の範囲第(1)項記載の電子ビーム露光用位置合せマークの形成方法。

(3) 前記第1のレジスト膜へ形成する第2の開口を2ケ所形成することにより前記半導体基板に凹部を2ケ所形成し、この凹部とこの2ケ所の凹部に挟まれた除去されない前記半導体基板とにより凸状の位置合せマークを形成することを特徴とする特許請求の範囲第(1)項記載の電子ビーム露光用位置合せマークの形成方法。

3.　発明の詳細な説明

[illegible]

本発明は半導体装置[illegible]

ム露光用位置合せマークの形成方法に関する。

（従来の技術）

[illegible]

寸法は著しく微細化されており、特に砒化ガリウム（GaAs）等の化合物半導体を用いたマイクロ波半導体装置の最小ゲート電極寸法はすでに0.25μmに達している。このような微細パターンの加工方法としては、電子ビームを用いた電子ビーム露光技術が広く採用されている。

電子ビーム露光で半導体基板にパターンを形成するために必要な位置合せマークは、半導体基板上に断面形状が凹状あるいは凸状、平面形状が十字形あるいはL字形のパターンを使用することが多い。この位置合せマークの形成条件によつて検出位置精度及び検出信号のS／N比が大幅に左右される。電子ビーム露光用位置合せマークに対して要求される条件はマークのエッジ部がシャープに切り立つていることや凹状あるいは凸状のマークの表面が平坦であることが最も重要である。

しかし電子ビーム露光は、露光に長時間要するため通常の光露光に比べてスループットが悪く半導体装置を製造するに際し、最も加工精度が要求される工程にのみ使用されることが多い。例えばGaAsFETを用いたショットキ障壁型電界効果トランジスタ（MESFET）では、ゲート電極のパターン形成に電子ビーム露光を用い、他の工程は光露光でパターン形成を行うことが一般的である。

MESFETの特性はゲート電極の寸法とオーミック電極であるソース電極及びドレイン電極との距離によつて大きな影響を受ける。したがつて、MESFETのゲート電極はオーミック電極に対して精度よく位置合せを行なわなければならない。このためMESFETに用いられる電子ビーム露光用位置合せマークはオーミック電極の形成と同時に形成されるのが望ましい。

しかしながら、MESFETのオーミック電極は一般にNiとAuGeからなる合金が用いられ半導体基板とのオーミック接触を得るために450℃以上の高温で合金化処理が行なわれる。このため電子ビーム露光用位置合せマークをNiとAuGeにより形成した場合には、オーミック電極の合金化処理のために位置合せマークのエッジ部の劣化及び表面の平坦性を著しく損ねてしまう。

したがつてオーミック電極と同時に電子ビーム露光用位置合せマークを形成しても電子ビーム照射によつて得られる位置検出精度や検出信号のS／N比は要求される値に対して不十分である。加えて合金化後の位置合せマークの表面状態はNiとAuGeのわずかな組成の違い及び合金化の際の温度、時間等の条件が多少変化するだけできつたく変わつた状態となり、ひどい場合には検出信号の雑音成分が多すぎてマーク検出不能となる場合もある。

またオーミック電極と電子ビーム用位置合せマークとを別々にパターニングし、電子ビーム用

[illegible]

ト電極の位置が設計値からずれてしまいMESFETの特性変動を引き起こしてしまう。

[illegible]

位置合せマークの形成方法では、オーミック電極の形成の際の熱処理工程により位置合せマークが変形してゲート電極の位置合せを正確にすることができなかつた。そこで本発明ではこのような欠点を排除し、ゲート電極の正確な位置合せを行なうことができる位置合せマークを形成することを目的とする。

〔発明の構成〕

（問題点を解決するための手段）

上記目的を達成するために本発明の電子ビーム露光用位置合せマークの形成方法では、半導体基板上にオーミック電極用の第1の開口と位置合せマーク形成用の第2の開口を有した薄膜を形成

[illegible]

位置合せマークを形成するものである。

（作用）

[illegible]

去することにより半導体基板に段差を形成し、この段差を位置合せマークとするために、オーミック電極形成時の合金化処理に伴う熱処理に対して、半導体基板の熱変形が起こりにくいので、位置合せマークが変形しない。又、位置合せマークの形成位置をオーミック電極の形成位置の決定と同時に行うために位置合せマークをターゲットとしてゲート電極を形成する場合、オーミック電極とゲート電極の位置ずれが無くなる。

（実施例）

以下本発明の一つの実施例について図面を参照して説明する。第1図(a)～(e)は本発明の電子ビーム露光用位置合せマークの形成方法の一実施例についてMESFETの製造方法を例に示した図である。第1図(a)に示すように半導体基板1、例えば半絶縁性GaAs基板上に活性層2を形成した後、この半導体基板1上に絶縁膜、例えばSiO_2膜3を3000Å、レジスト膜4を順次積層する。

次に第1図(b)に示すように、SiO_2膜3をエッチング除去するためにレジスト膜4に第1の開口5及び第2の開口6を形成する。ここで第1の開口5はオーミック電極であるソース電極及びドレイン電極を形成するために、レジスト膜4の活性層2が形成された部分に対応する位置に2ケ所形成する。又、第2の開口6は位置合せマークを形成するためにレジスト膜4の活性層が形成されない部分に対応する位置に1ケ所形成する。その後、レジスト膜4をマスクにして露出したSiO_2膜3を同時にエッチング除去する。

次に第1図(c)に示すように、Ni－AuGeで構成された金属膜を第1の開口5及び第2の開口6を通して活性層2及び半導体基板1上に2000Å被着する。ここで第1の開口を通して被着された金属膜はオーミック電極用金属膜7－1となり第2の開口を通して被着された金属膜は位置合せマーク用金属膜7－2となる。さらにリフトオフ法を用いて不要部分の金属膜をレジスト膜とともに除去する。

次に第1図(d)に示すように、新たにレジスト膜8を半導体基板1に塗布し、位置合せマーク用金属膜7－2を含む第3の開口を形成する。さらにこの第3の開口9内の位置合せマーク用金属膜7－2をエッチング除去して半導体基板1面を露出した後、SiO_2膜3をマスクとして半導体基板1の露出面をエッチングして凹状の位置合せマーク10を形成する。

次に第1図(e)に示すように、SiO_2膜3を剥離し合金化処理によってオーミック電極11を形成し、最後に電子ビーム露光によって位置合せマーク10をターゲットにゲート電極の位置合せを行ってゲート電極12を形成することによりMESFETが完成する。

このようにして得られた電子ビーム露光用位置

ート電極の良好な信号検出を行うことができる。又、オーミック電極を形成する過程においてオー

ミック電極に対する位置は設計値と殆ど同じにすることができる。

なお第1図の説明では、電子ビーム露光用位置合せマークの断面形状として凹状の例を説明したが、凸状の位置合せマークを形成することも可能である。すなわち第1の実施例の第1図(b)の工程において、第1の開口5を設けるのと同時にレジスト膜4の半導体基板1上の活性層2が形成されない部分に第2の開口6'を2ケ所設ける。次にこのレジスト膜4をマスクとしてSiO_2膜3をエッチング除去する。さらに金属膜を半導体基板1の全面に被着した後、リフトオフ法を用いてレジスト膜4と不要な金属膜を除去すると、第2図

次に第2図(b)に示すように、新たにレジスト

る。さらに第3の開口9′内の位置合せ用金属膜7－2′をエッチング除去して半導体基板1を露出した後、SiO_2膜3をマスクとして半導体基板1の露出面をエッチングすることにより2ケ所の凹部を形成する。ここでこの2ケ所の凹部は、凹部に挟まれたエッチングされない半導体基板1とにより擬似的に凸状の位置合せマーク10′を形成する。最後に第2図(c)に示すように凸状の位置合せマーク10′をターゲットにゲート電極の位置合せを行つてゲート電極12を形成する。

このようにして得られた凸状の位置合せマーク10′は、上記第1の実施例と同様にオーミック電極形成時の合金化処理に対して影響されることがないとともに、位置合せ精度が高くなる。

なお、上記第1の実施例及び第2の実施例において半導体基板1のエッチングの深さについては位置合せマーク検出のための電子ビーム照射の条件によつて決める必要があるが、0.3mm程度の比較的浅い場合でも十分な信号強度が得られる。また、SiO_2膜3の膜厚としてはオーミック電極用金属膜7をリフトオフする際のスペーサ膜としても使えるようにオーミック電極用金属膜と同じか、あるいはそれ以上の厚さが望ましい。

また、SiO_2膜は他の絶縁膜例えばSiOやSi_3N_4やAℓ，Auなどの金属膜及びこれらの組み合せであつてもよく、半導体基板も半絶縁性GaAs基板に限定されるものではない。また、オーミック電極用金属膜としてNi－AuGeを例にとつたが、Au－AuGe，Pt－AuGeでもよく、オーミック電極用金属の上部にAu-Pt-Tiからなるボンデイングパット用金属が被つていてもかまはない。さらに、電子ビーム露光に限定されず他の荷電ビーム露光、例えばイオンビーム露光においても適用できることは勿論である。

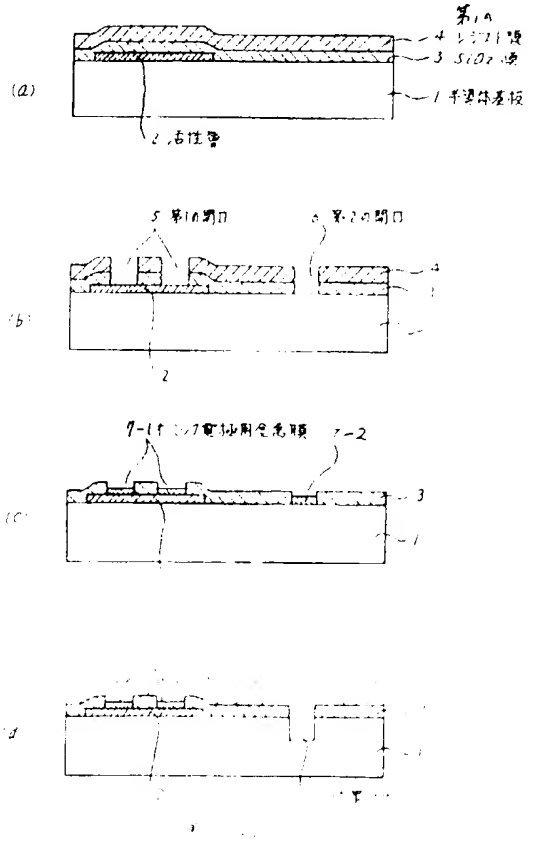
〔発明の効果〕

以上述べたように本発明によれば、位置合せマークを直接半導体基板に形成するので、オーミック電極形成時の合金化処理に伴う熱処理工程による位置合せマークの変形が行こらない。したがつて、位置検出精度が高く、雑音成分が少ない検出信号が得られ良好な電子ビーム露光用位置合せマークを形成することができる。

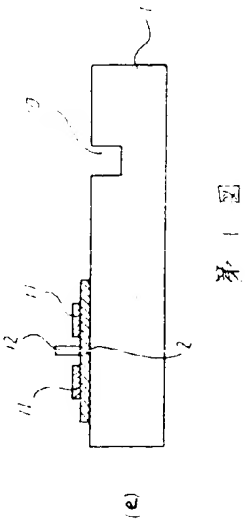
4. 図面の簡単な説明

第1図(a)乃至第1図(e)は本発明の一実施例を示す工程断面図，第2図(a)乃至第2図(c)は本発明の他の実施例を示す工程断面図である。

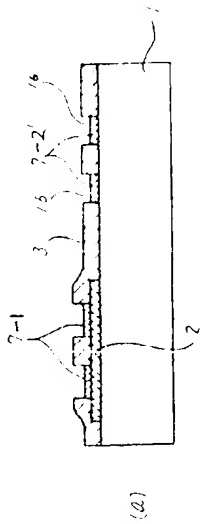
1…半導体基板、2…活性層、3…SiO_2膜、4…第1のレジスト膜、5…第1の開口、6…第2の開口、7－1…オーミック電極用金属膜、7－2，7－2′…位置合せマーク用金属膜、8…第2のレジスト膜、9，9′…第3の開口、10，10′…位置合せマーク。



代理人　弁理士　　則　近　憲　佑



第1図



第2図